CLAIMS

We Claim:

1 A method for reducing intersymbol interference in a stream of data bits to be transmitted over a transmission medium, comprising:

(a) delaying a reference clock to produce a phase delayed clock that produces an edge on sub-bit boundaries; and

(b) inputting the phase delayed clock and the data bits into a digital filter in order to perform equalization on the data bits, wherein the phase delayed clock causes the digital filter to perform partial clock switching, such that equalization is performed on the data bits on sub-bit boundaries.

2 The method of claim 1 wherein the digital filter produces an equalized output signal having a frequency response of aSinc(f)+bSinc(2f).

3 The method of claim 2 further including the step of: inputting a driver clock to the digital filter along with the phase delayed clock, wherein the phase delayed clock appears at an output at a predetermined intermediate time of the driver clock.

4 The method of claim 3 wherein each of the data bits has a sample period of time duration T, and the delay of the phase delayed clock may be set at any

portion of the time duration T, including 3/4, 1/2, 1/3, and 1/4 of the time duration T.

5 The method of claim 4 further including the step of: delaying the reference clock using a partial clock switching circuit.

6 The method of claim 5 wherein the partial clock switching circuit comprises a phased locked loop (PLL) coupled to a set of n PLL variable delay cells, wherein the number of delay cells controls an amount of delay of the input reference clock.

7 The method of claim 6 wherein the digital filter includes a finite impulse response (FIR) filter.

8 The method of claim 7 wherein the FIR filter includes a plurality of Z-domain delay blocks, gain stages, and summing junctions.

9 The method of claim 8 wherein the transmission medium comprises a serial link.

10 A system for reducing intersymbol interference in a stream of data bits to be transmitted over a transmission medium, comprising:

(a) a phase delayed clock generated from a reference clock that produces an edge on sub-bit boundaries; and

(b) a digital filter coupled to the phase delayed clock for performing equalization on the data bits, wherein the phase delayed clock causes the digital filter to perform partial clock switching, such that equalization is performed on the data bits on sub-bit boundaries.

11 The system of claim 10 wherein the digital filter produces an equalized output signal having a frequency response of aSinc(f)+bSinc(2f).

12 The system of claim 11 wherein a driver clock is input to the digital filter along with the phase delayed clock, wherein the phase delayed clock appears at an output at a predetermined intermediate time of the driver clock.

13 The system of claim 12 wherein each of the data bits has a sample period of time duration T, and the delay of the phase delayed clock may be set at any portion of the time duration T, including 3/4, 1/2, 1/3, and 1/4 of the time duration T.

14 The system of claim 13 wherein the reference clock is delayed using a partial clock switching circuit.

15 The system of claim 14 wherein the partial clock switching circuit comprises a phased locked loop (PLL) coupled to a set of n PLL variable delay cells, wherein the number of delay cells controls an amount of delay of the input reference clock.

16 The system of claim 15 wherein the digital filter includes a finite impulse response (FIR) filter.

17 The system of claim 16 wherein the FIR filter includes a plurality of Z-domain delay blocks, gain stages, and summing junctions.

18 The system of claim 17 wherein the transmission medium comprises a serial link.